SPECIFICATION AMENDMENTS

Please amend the Specification as follows.

[0020] The elements of processing blade 400 are interconnected as follows. Processor(s) 415 are communicatively coupled to firmware unit 420, system memory 425, hard disk(s) 430, and communication links 435A and 435B via system bus 440 to send and to ~~received~~ receive instructions thereto/therefrom. In one embodiment, firmware unit 420 is a flash memory device. In other embodiments, firmware unit 420 includes any one of read only memory ("ROM"), programmable ROM, erasable programmable ROM, electrically erasable programmable ROM, or the like. In one embodiment, system memory 425 includes random access memory ("RAM"). In one embodiment, communication links 435A and 435B include network interface cards ("NICs"). Hard disk(s) 430 may optionally include one or more of an integrated drive electronic ("IDE") hard disk, an enhanced IDE ("EIDE") hard disk, a redundant array of independent disks ("RAID"), a small computer system interface ("SCSI") hard disk, and the like.

[0031] Returning to FIG. 6, in a decision block 635 it is determine[[d]] whether processing blade 400 includes more than one processor 415. If processing blade 400 includes multiple processor(s) 415, the processors are allocated to one of two groups—application processors ("APs") and a boot-strap processor ("BSP"). Although processing blade 400 may include several AP processors, only one of processor(s) 415 is a BSP at any given time. The current BSP is responsible for servicing the MMI. If processing blade 400 includes multiple processors 415, then process 600 continues to a process block 640.

[0036] In a process block 660, VMC 405 generates one or more command packets to transmit to CMM 410 based on the parsed interrupt data. The command packet(s) contain the requisite requests/information to enable software entity 705 to accomplish the desired task. In a decision block 665, VMC 405 waits until CMM 410 is available. If CMM 410 is currently busy performing other management tasks, VMC 405 manages the timeout in a process block 667. Managing a timeout may include simply waiting a predetermine[[d]] period of time and then checking to see if CMM 405 is available or other known techniques for managing timeouts.

[0037] Once CMM 410 is available for communication with VMC 405, VMC 405 transmits the command packet(s) to CMM 410, in a process block 670. In a decision block 675 and a process block 677, VMC 405 waits for a response from CMM 410 and manages an[[y]] timeouts that may occur, as described above. In a process block 680, CMM 410 returns results to VMC 405 in response to the command packet(s) transmitted in process block 670. The returned results may simply indicate that software entity 705 has been granted access to the requested shared resource, may indicate that software entity 705 has been denied access to the requested shared resources, may include an error code or may be other instructions, commands, or information from CMM 410 relating to any one of the management tasks performed by CMM 410.

[0039] In a process block 690, VMC 405 clears interrupt register 720 or returns it to a default value. Although process 600 illustrates process block 690 occurring subsequently to VMC 405 updating shared memory 710, it should be appreciated that other embodiment[[s]] of the present invention may include clearing interrupt register 720 prior to or concurrently with updating shared memory 710.